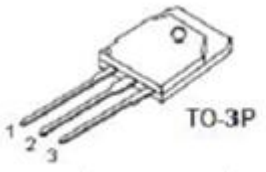
1. Description

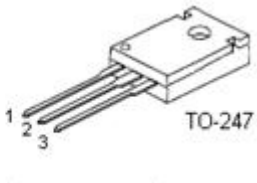
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge to pology.

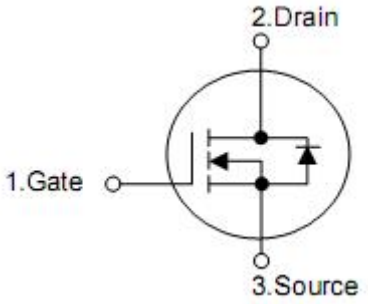
2. Features

- 9A, 900V, $R_{DS(on)}$=1.12Ω @ V_{GS}=10 V
- Low gate charge (typical 70 nC)
- Low Crss (typical 14pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant

3. Pin configuration







Pin	Function
1	Gate
2	Drain
3	Source

4. Absolute maximum ratings

(T_C= 25 ºC , unless otherwise specified)

Parameter		Symbol	Ratings	Units
Drain-source voltage		V_{DSS}	900	V
Drain current	T_C=25°C	I_D	9.0	A
	T_C=100°C		5.7	A
Drain current (note1)		I_{DM}	36	A
Gate-source Voltage		V_{GSS}	± 30	V
Single pulsed avalanche energy (note2)		E_{AS}	900	mJ
Avalanche current (note1)		I_{AR}	9.0	A
Repetitive avalanche energy (note1)		E_{AR}	28	mJ
Peak diode recovery dv/dt (note 3)		dv/dt	4.0	V/ns
Power dissipation	T_C=25°C	P_D	280	W
	Derate above 25°C		2.22	W/°C
Operating and storage temperature range		T_J, T_{STG}	-55 to +150	°C
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		T_L	300	°C

5. Thermal characteristics

Parameter	Symbol	Typ	Max	Units
Thermal resistance, junction-to-case	$R_{\theta JC}$	-	0.45	°C/W
Thermal resistance, case-to-sink	$R_{\theta CS}$	0.24	-	°C/W
Thermal resistance, junction-to-ambient	$R_{\theta JA}$	-	40	°C/W

6. Electrical characteristics

(T_C=25°C,unless otherwise notes)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Off characteristics							
Drain-source breakdown voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	900	-	-	V
Zero gate voltage drain current		I_{DSS}	V_{DS}=900V,V_{GS}=0V	-	-	10	μA
			V_{DS}=720V,T_C=125°C	-	-	100	μA
Gate-body leakage current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V	-	-	100	nA
	Reverse		V_{GS}=-30V,V_{DS}=0V	-	-	-100	nA
Breakdown voltage temperature coefficient		$\triangle BV_{DSS}/\triangle T_J$	I_D=250μA Referenced to 25°C	-	0.9	-	V/°C
On characteristics							
Gate threshold voltage		$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	3.0	-	5.0	V
Static drain-source on-resistance		$R_{DS(on)}$	V_{GS}=10V,I_D=4.5A	-	1.12	1.4	Ω
Forward transconductance		g_{FS}	V_{DS}=40V,I_D=4.5A (note4)	-	9.0	-	S
Dynamic characteristics							
Input capacitance		C_{ISS}	V_{DS}=25V,V_{GS}=0V, f=1MHz	-	2780		pF
Output capacitance		C_{OSS}		-	228		pF
Reverse transfer capacitance		C_{RSS}		-	28		pF
Switching characteristics							
Turn-on delay time		$t_{D(ON)}$	V_{DD}=450V,I_D=9.0A, R_G=25Ω (note4, 5)	-	55		ns
Rise time		t_R		-	130		ns
Turn-off delay time		$t_{D(OFF)}$		-	110		ns
Fall time		t_F		-	80		ns
Total gate charge		Q_G	V_{DS}=720V, I_D=9.0A, V_{GS}=10V (note4, 5)	-	70		nC
Gate-source charge		Q_{GS}		-	13.5	-	nC
Gate-drain charge		Q_{GD}		-	27	-	nC
Drain-source diode characteristics and maximum ratings							
Maximum continuous drain-source diode forward current		I_S		-	-	9.0	A
Maximum pulsed drain-source diode forward current		I_{SM}		-	-	36.0	A
Drain-source diode forward voltage		V_{SD}	V_{GS}=0V,I_S=9.0A	-	-	1.4	V
Reverse recovery time		t_{RR}	V_{GS}=0V,I_S=9.0A, dI_F/dt=100A/μs (note 4)	-	850	-	ns
Reverse recovery charge		Q_{RR}		-	10	-	μC

Note: 1. Repetitive rating : pulse width limited by maximum junction temperature
2. L=21mH, I_{AS}= 9.0A, V_{DD}=50V, R_G=25Ω, starting T_J=25°C
3. I_{SD}≤9.0A, di/dt≤200A/μs, V_{DD}≤BV_{DSS}, Starting T_J=25°C
4. Pulse test : pulse width≤300μs, duty cycle≤2%
5. Essentially independent of operating temperature

7. Test circuits and waveforms

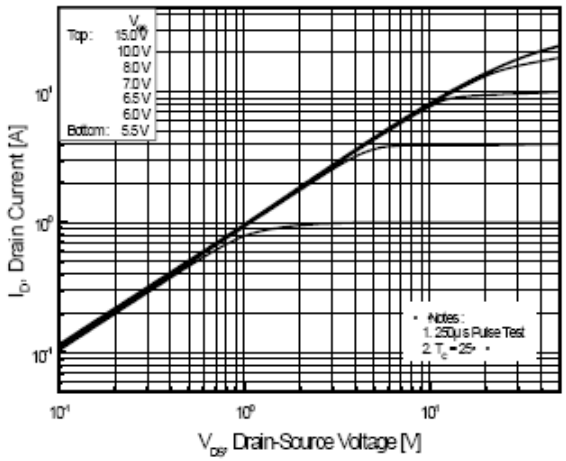


Figure 1. On-Region Characteristics

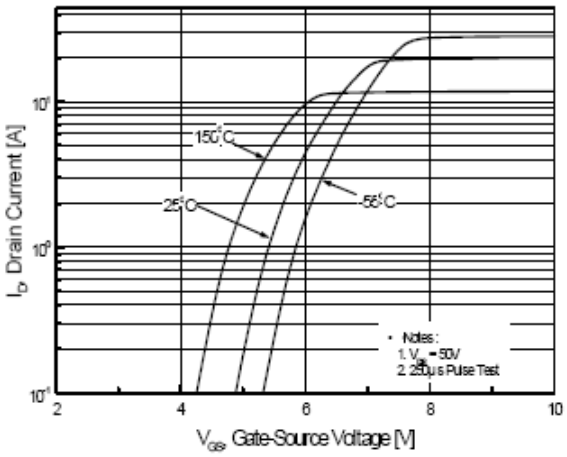


Figure 2. Transfer Characteristics

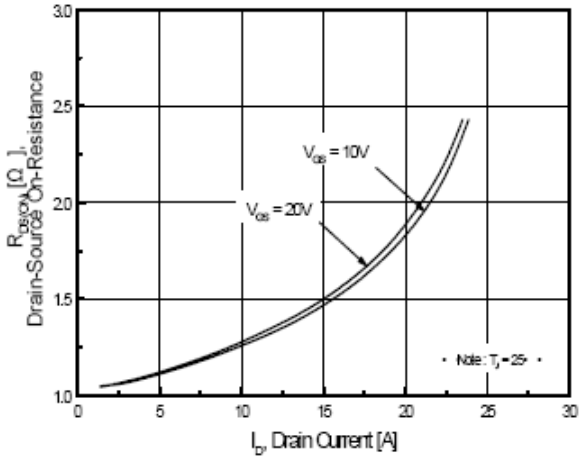


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

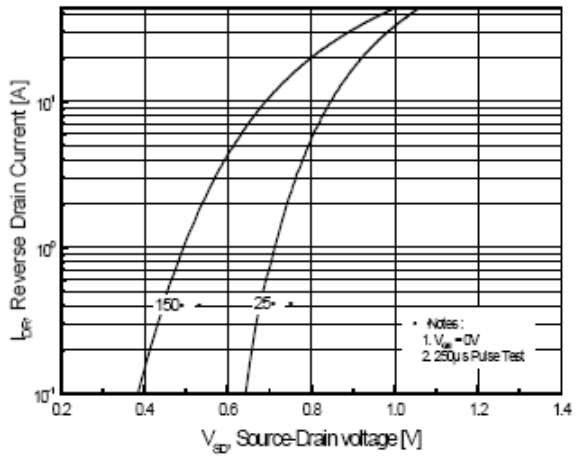


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

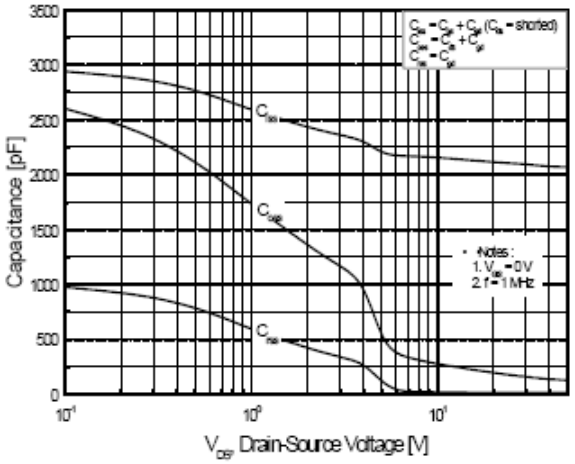


Figure 5. Capacitance Characteristics

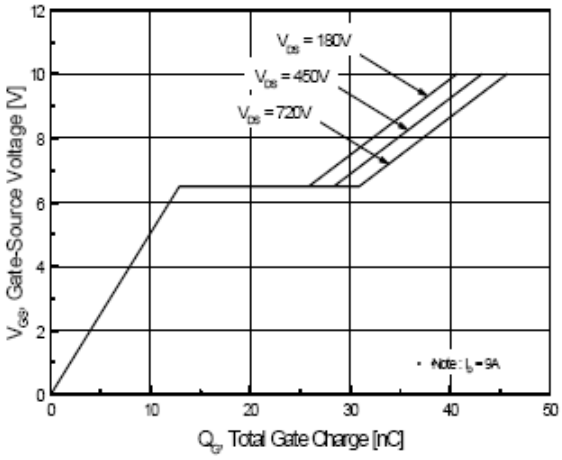


Figure 6. Gate Charge Characteristics

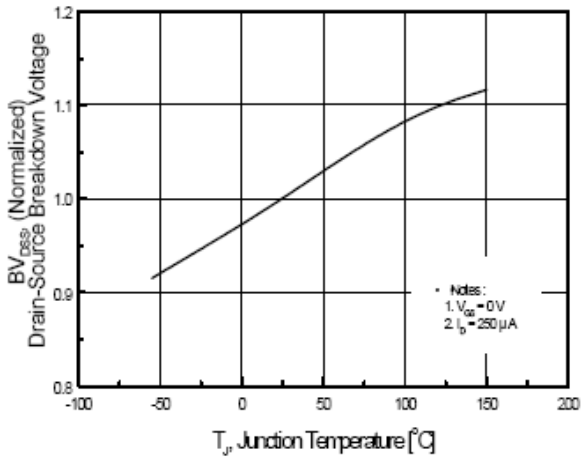


Figure 7. Breakdown Voltage Variation vs. Temperature

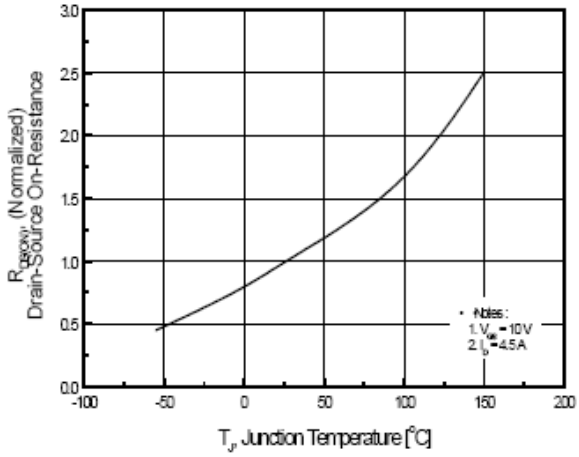


Figure 8. On-Resistance Variation vs. Temperature

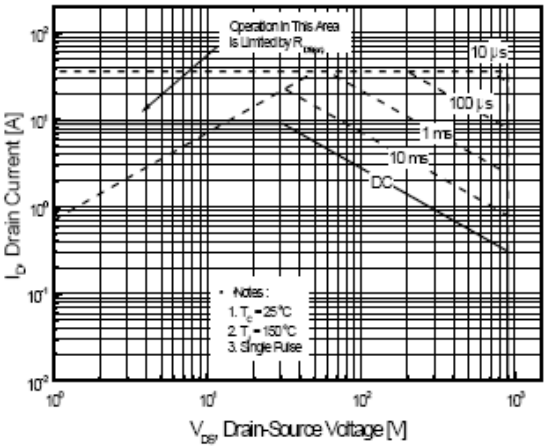


Figure 9. Maximum Safe Operating Area

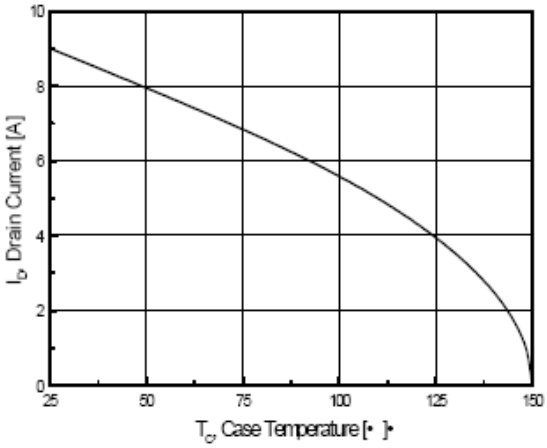


Figure 10. Maximum Drain Current vs. Case Temperature

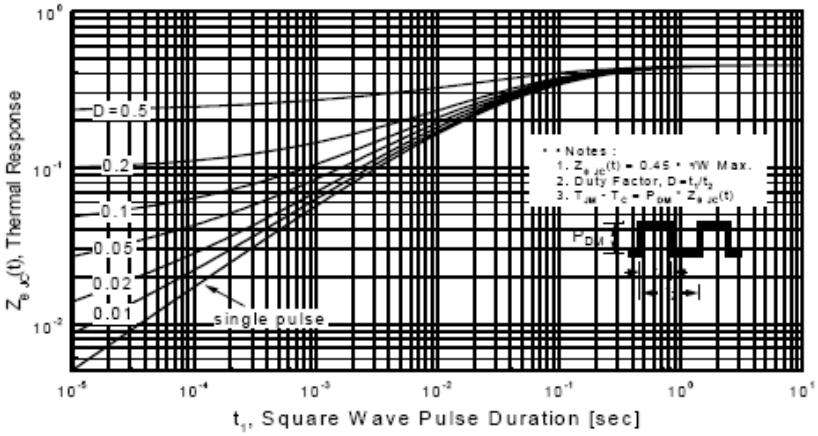
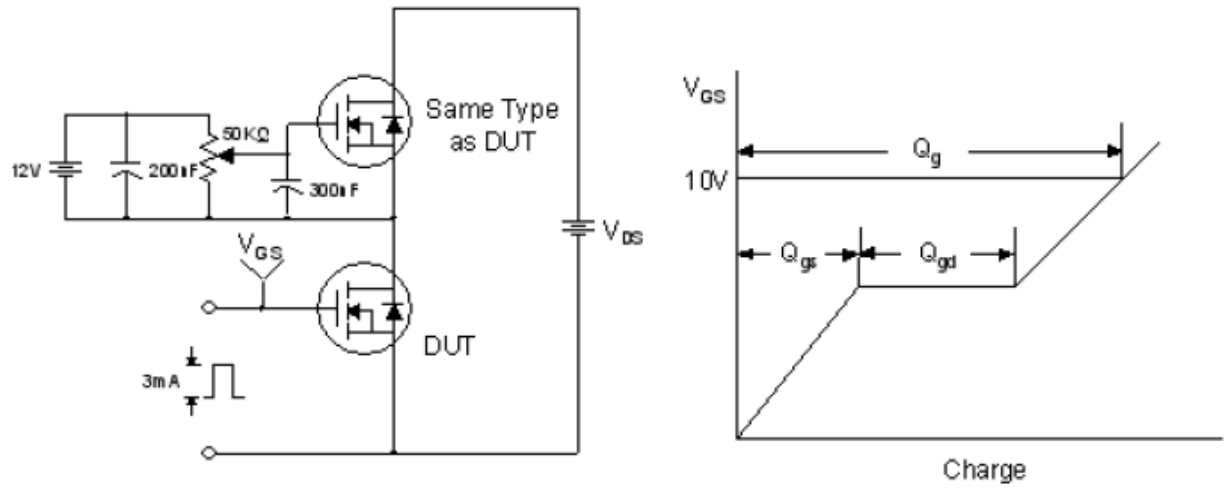
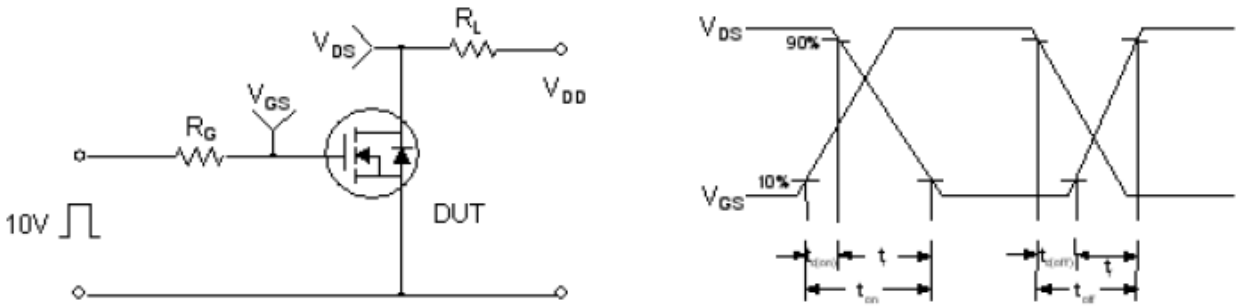


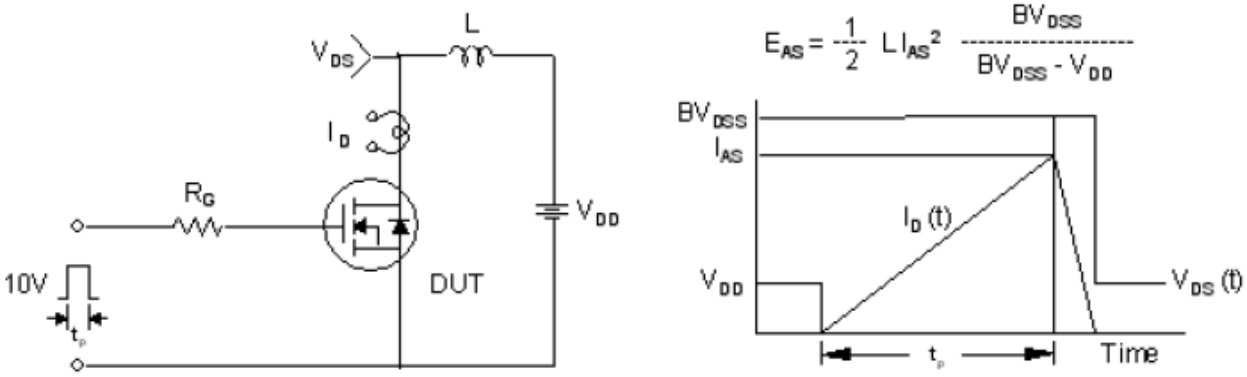
Figure 11. Transient Thermal Response Curve



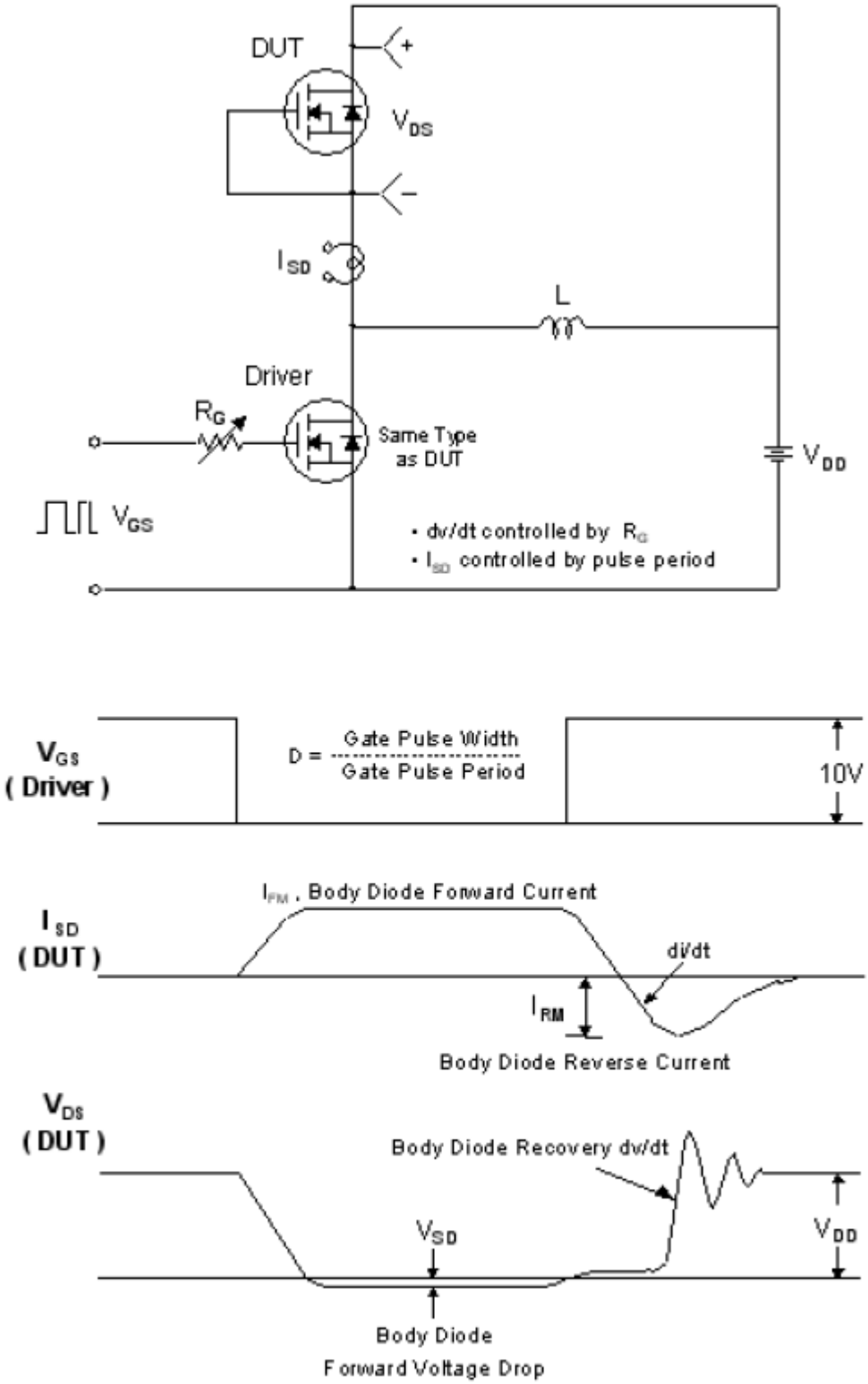
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms