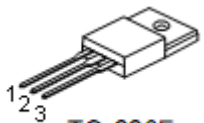
1. Description

This Power MOSFET is produced using KIA semi`s advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

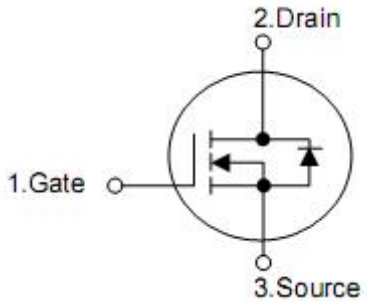
2. Features

- $R_{DS(on)}$=1.15Ω @ V_{GS}=10V
- Low gate charge (typical 22nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

3. Pin configuration



TO-220F



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Absolute maximum ratings

(T_C= 25 ºC , unless otherwise noted)

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	600	V
Gate-source voltage		V_{GSS}	±30	V
Drain current continuous	T_C=25ºC	I_D	7.0*	A
	T_C=100ºC		4.2*	A
Drain current pulsed (note1)		I_{DM}	28*	A
Avalanche energy	Repetitive (note1)	E_{AR}	17.6	mJ
	Single pulse (note2)	E_{AS}	280	mJ
Peak diode recovery dv/dt (note3)		dv/dt	4.5	V/ns
Total power dissipation	T_C=25 ºC	P_D	39	W
	derate above 25 ºC		0.31	W/ºC
Operating and storage temperature range		T_J, T_{STG}	-55~+150	ºC
Maximum lead temperature for soldering purposes, 1/8″ from case for 5 seconds		T_L	300	ºC

* Drain current limited by maximum junction temperature

5. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance, Junction-ambient	R_{thJA}	62.5	ºC/W
Thermal resistance, case-to-sink typ.	R_{thCS}	-	ºC/W
Thermal resistance, Junction-case	R_{thJC}	3.2	ºC/W

6. Electrical characteristics

(T_C=25°C,unless otherwise noted)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics							
Drain-source breakdown voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	600	-	-	V
Zero gate voltage drain current		I_{DSS}	V_{DS}=600V ,V_{GS}=0V	-	-	1	μA
			V_{DS}=480V ,T_C=125ºC	-	-	10	μA
Gate-body leakage current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V	-	-	100	nA
	Reverse		V_{GS}=-30V,V_{DS}=0V	-	-	-100	nA
Breakdown voltage temperature coefficient		△BV_{DSS}/△T_J	I_D=250μA,referenced to 25°C	-	0.6	-	V/°C
On characteristics							
Gate threshold voltage		$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0	-	4.0	V
Static drain-source on-resistance		$R_{DS(on)}$	V_{DS}=10V,I_D=3.5A	-	1.15	1.4	Ω
Dynamic characteristics							
Input capacitance		C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1MHz	-	1020	-	pF
Output capacitance		C_{oss}		-	90	-	pF
Reverse transfer capacitance		C_{rss}		-	10.5	-	pF
Switching characteristics							
Turn-on delay time		$t_{d(on)}$	V_{DD}=300V,I_D=7A, R_G=25Ω (note4,5)	-	15	-	ns
Rise time		t_r		-	9	-	ns
Turn-off delay time		$t_{d(off)}$		-	83	-	ns
Fall time		t_f		-	21	-	ns
Total gate charge		Q_g	V_{DS}=480V,I_D=7A , V_{GS}=10V (note4,5)	-	22	-	nC
Gate-source charge		Q_{gs}		-	5	-	nC
Gate-drain charge		Q_{gd}		-	8	-	nC
Drain-source diode characteristics and maximum ratings							
Drain-source diode forward voltage		V_{SD}	V_{GS}=0V,I_{SD}=7A	-	-	1.4	V
Continuous drain-source current		I_{SD}		-	-	7	A
Pulsed drain-source current		I_{SM}		-	-	28	A
Reverse recovery time		t_{rr}	V_{GS}=0V,I_{SD}=7A dI_F/dt=100A/μs (note4)	-	405	-	ns
Reverse recovery charge		Q_{rr}		-	3.3	-	μC

Note:1. Repetitive rating: pulse width limited by maximum junction temperature

2. L=9mH,I_{AS}=7A,V_{DD}=50V,R_G=25Ω,staring T_J=25ºC

3. I_{SD}≤7.0A,di/dt≤200A/μs, V_{DD}≤BV_{DSS}, staring T_J=25 ºC

4. Pulse test: pulse width≤300μs,duty cycle≤2%

5. Essentially independent of operating temperature

7. Test circuits and waveforms

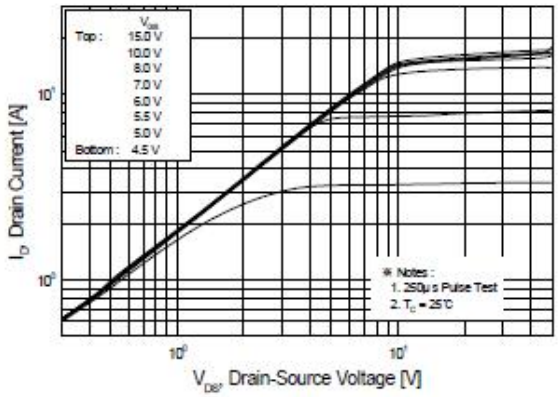


Figure 1. On-Region Characteristics

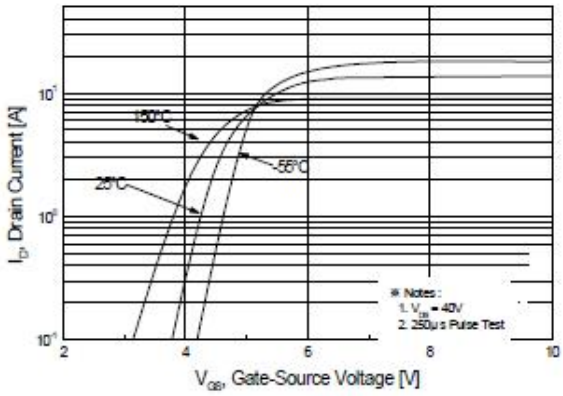


Figure 2. Transfer Characteristics

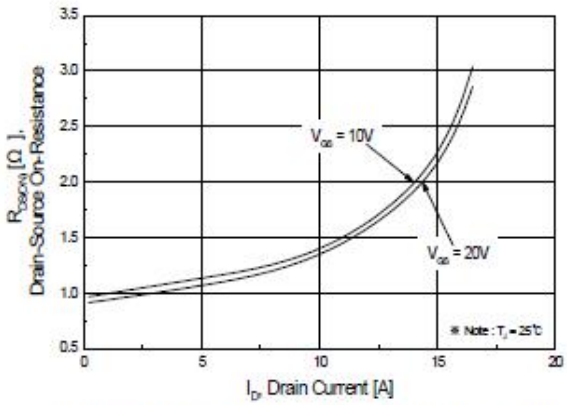


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

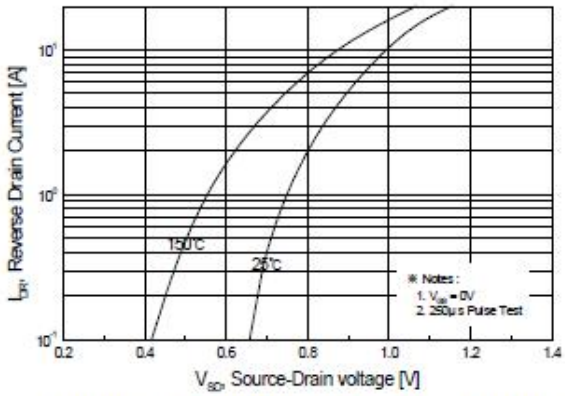


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

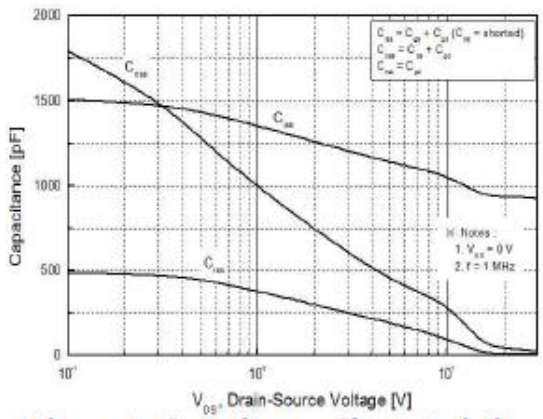


Figure 5. Capacitance Characteristics

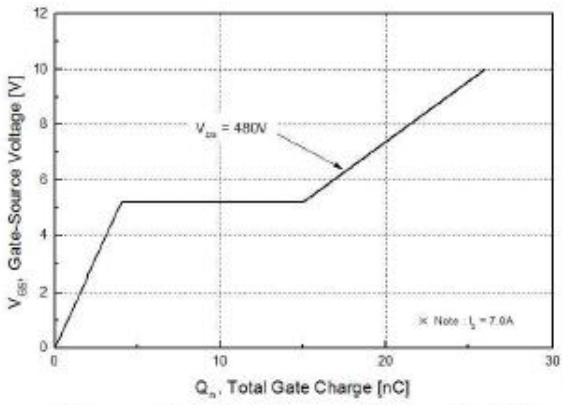


Figure 6. Gate Charge Characteristics

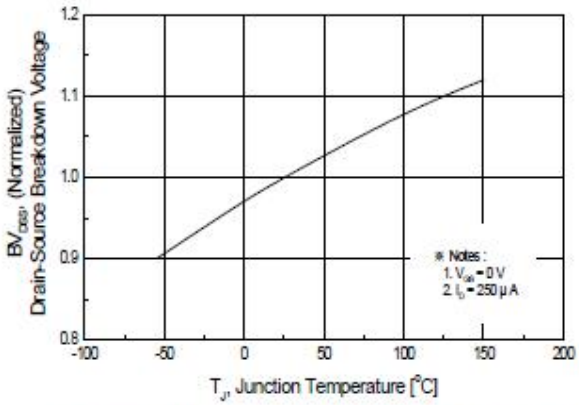


Figure 7. Breakdown Voltage Variation vs Temperature

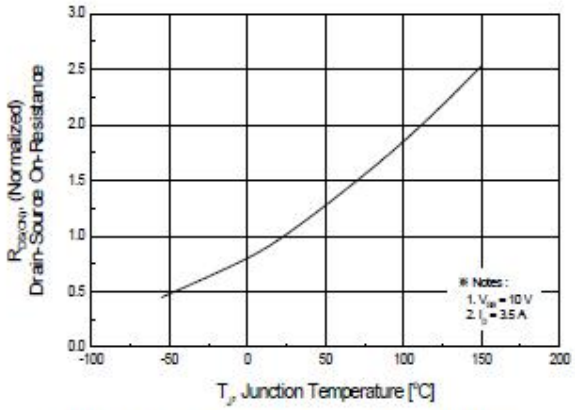


Figure 8. On-Resistance Variation vs Temperature

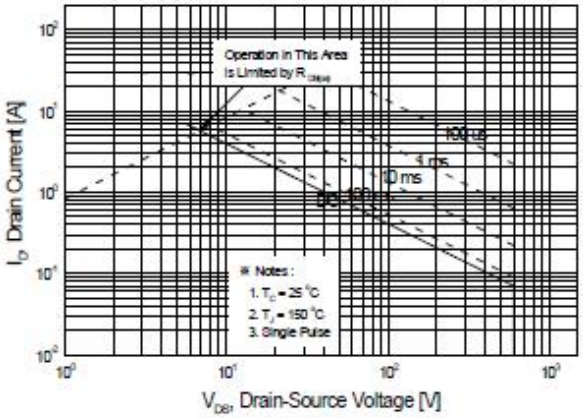


Figure 9 Maximum Safe Operating Area

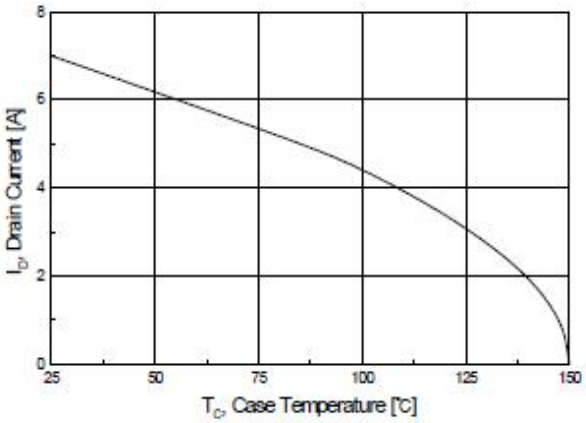


Figure 10. Maximum Drain Current vs Case Temperature

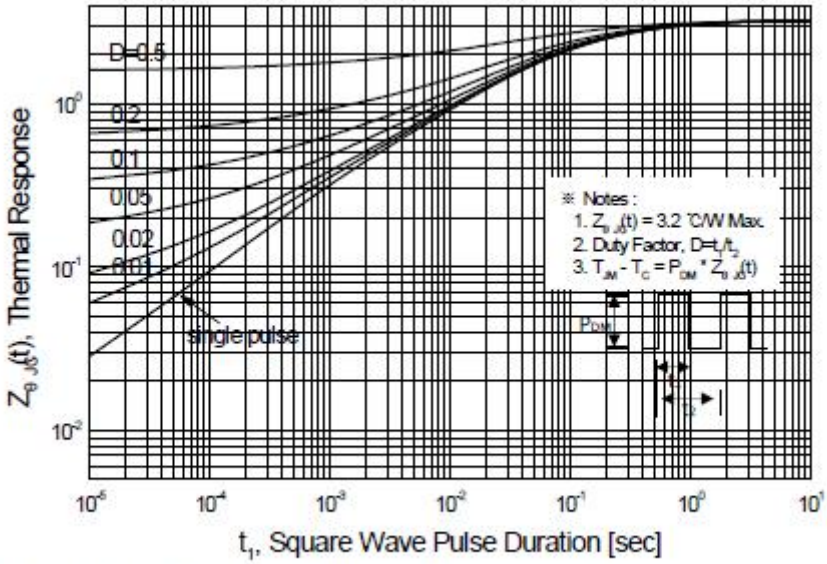
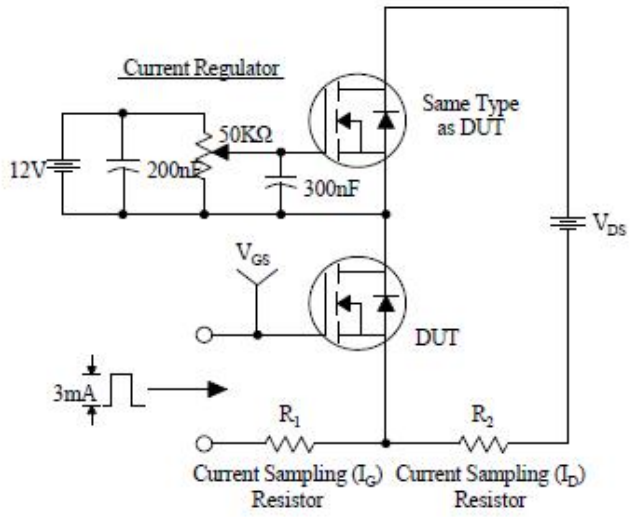
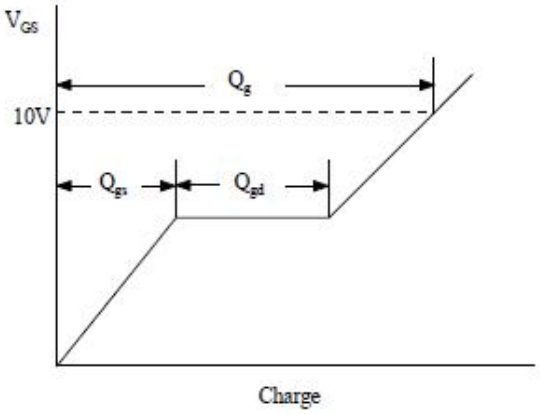


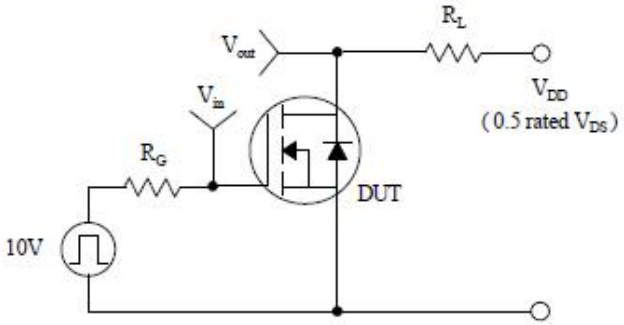
Figure 11 Transient Thermal Response Curve

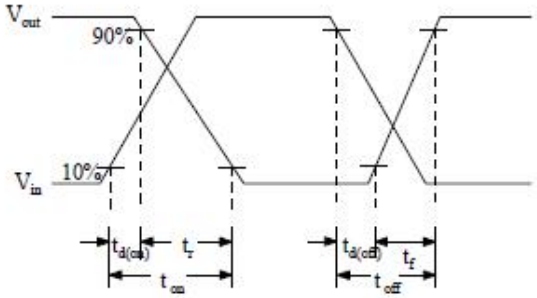
Gate Charge Test Circuit & Waveform



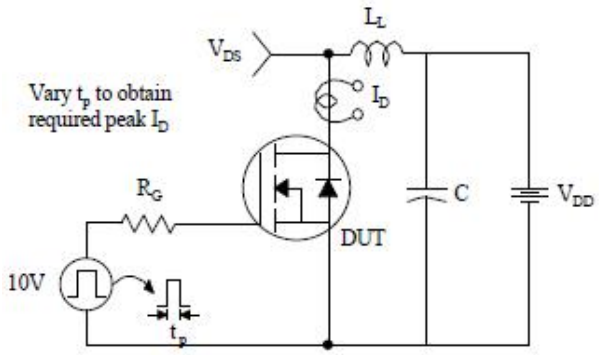


Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$